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Tomaoka et al
JP 1999-026705 (8728-457) (MU)

FIG. 1

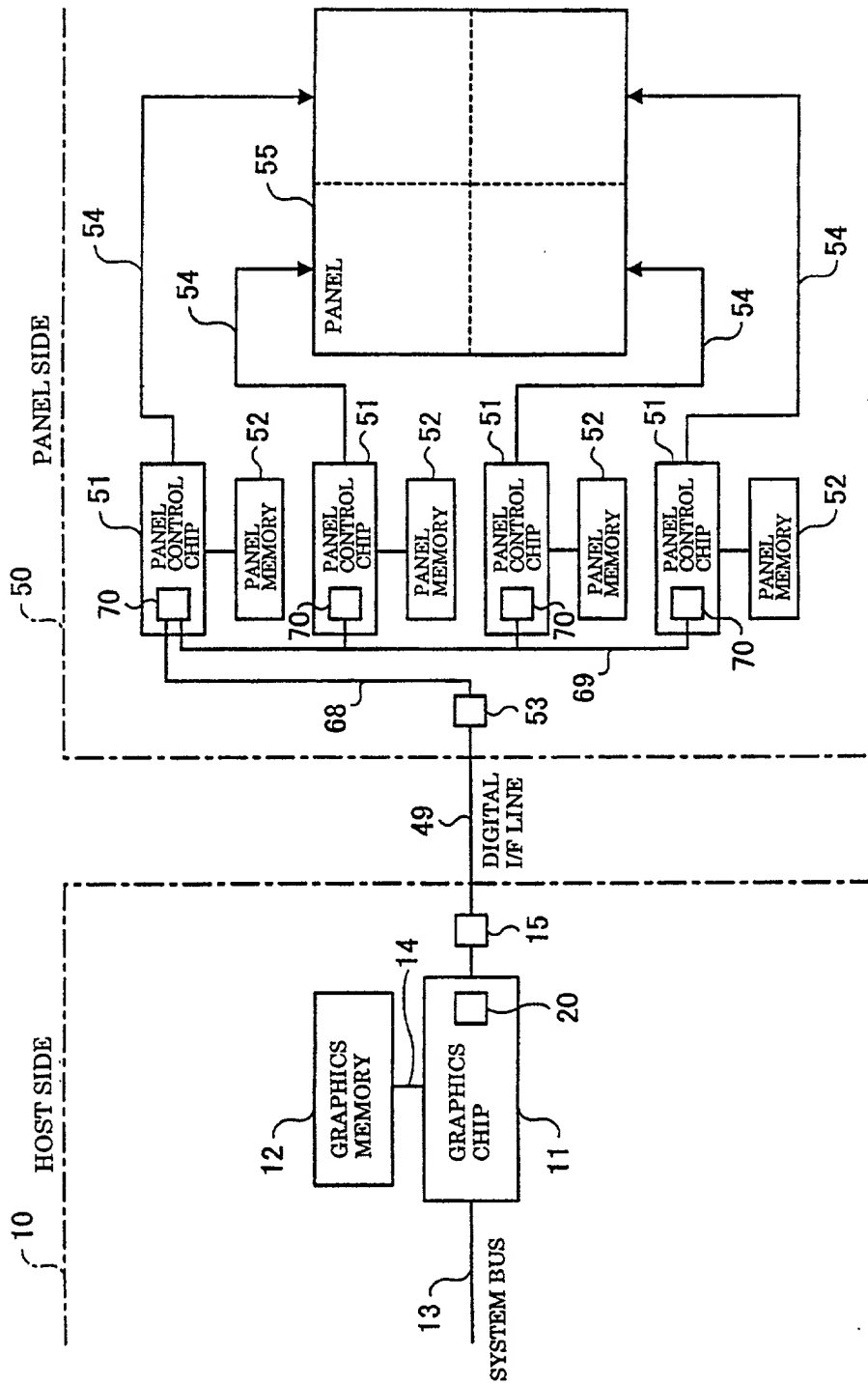


FIG. 2

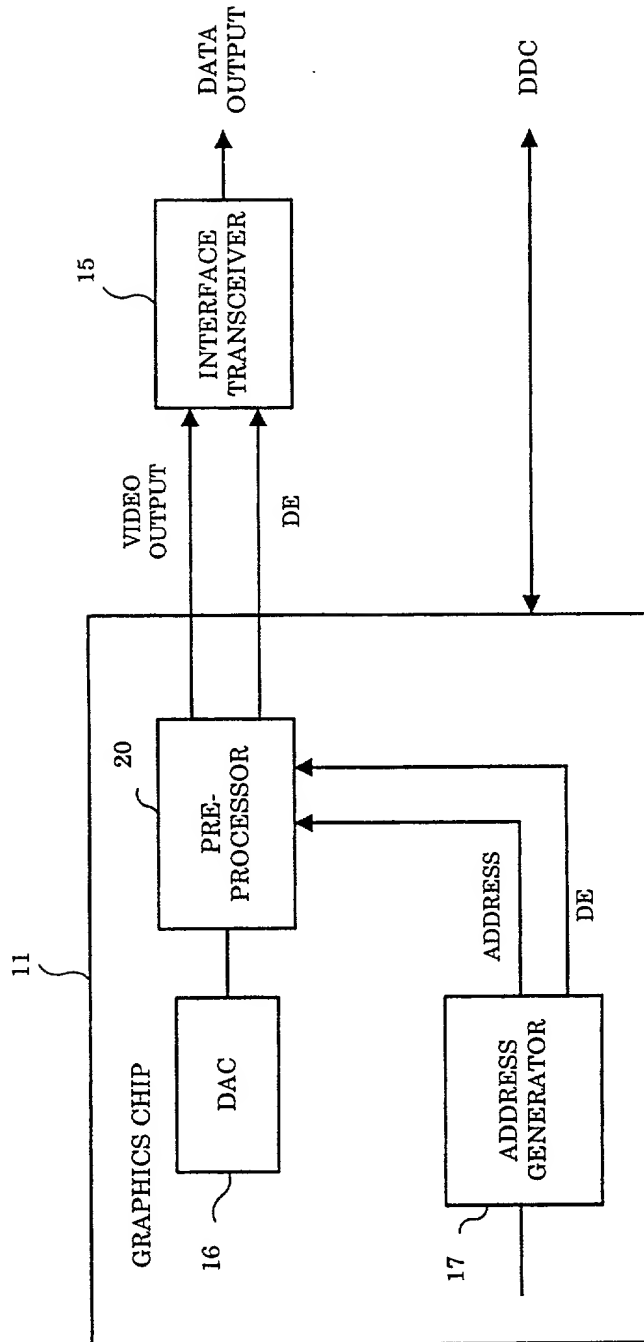
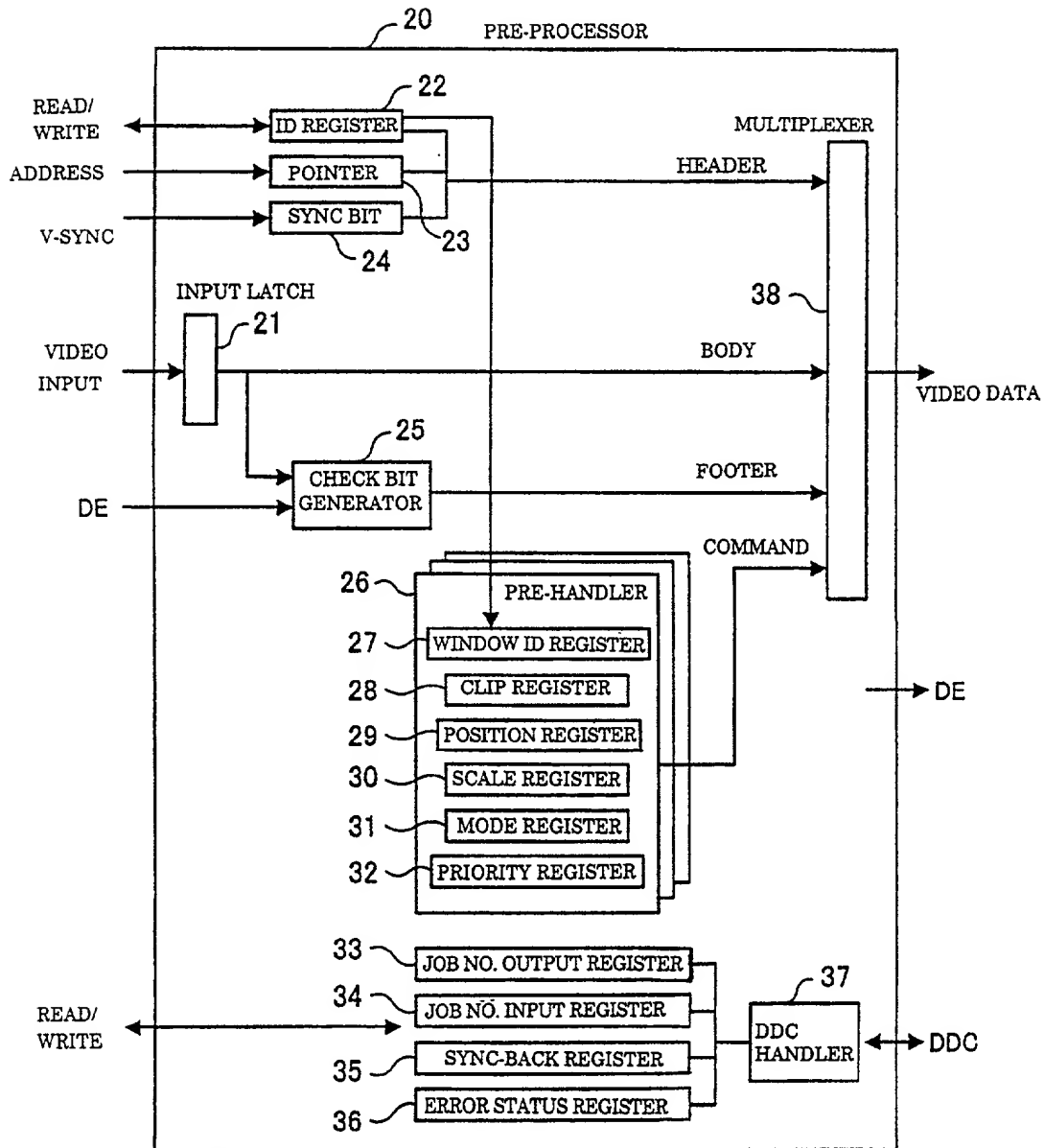


FIG. 3



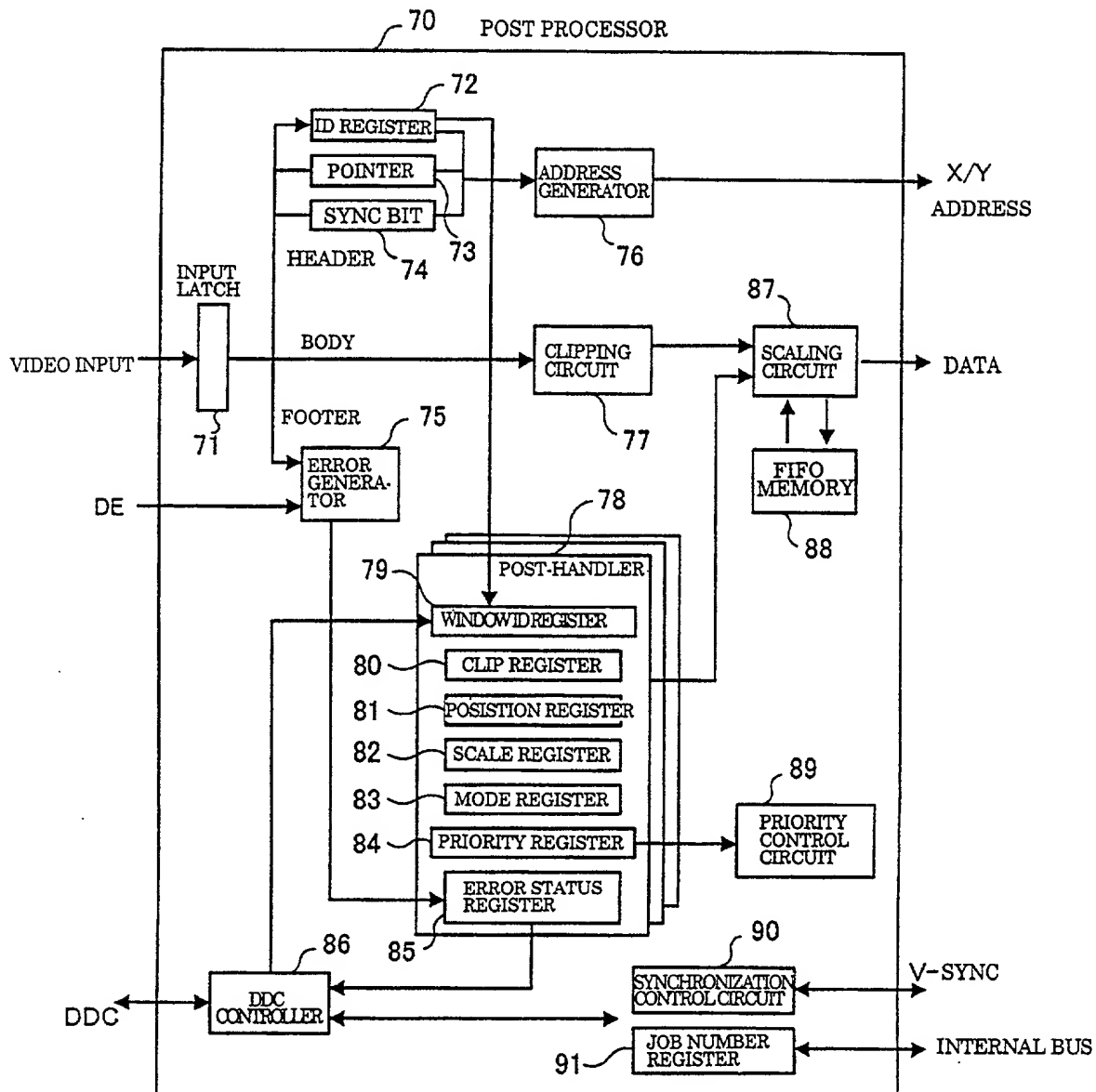
Demographic Data		Clinical Data		Outcome Data	
Variable	Value	Variable	Value	Variable	Value
Age (years)	65.2	Gender	Male	Survived (%)	85.2
Weight (kg)	78.5	Height (cm)	175.3	Discharge Status	Discharged
Smoking Status	Smoker	Diagnosis	Myocardial Infarction	Follow-up (months)	12.5
Medical History	Hypertension	Treatment	Aspirin	Quality of Life Score	7.8
Lab Results	Cholesterol	Medication	Statins	Readmission Rate	15.3
Comorbidities	Diabetes	Prognosis	Good	Patient Satisfaction	92.1
Social Support	Family	Healthcare Access	Good	Healthcare Costs	\$12,500
Insurance Status	Private	Healthcare Quality	High	Healthcare Equity	High
Healthcare Utilization	Emergency	Healthcare Innovation	High	Healthcare Sustainability	High
Healthcare Policy	Universal	Healthcare Research	High	Healthcare Education	High
Healthcare Regulation	Strict	Healthcare Standards	High	Healthcare Accreditation	High
Healthcare Funding	Government	Healthcare Infrastructure	High	Healthcare Workforce	High
Healthcare Technology	Advanced	Healthcare Innovation	High	Healthcare Research	High
Healthcare Policy	Universal	Healthcare Regulation	Strict	Healthcare Funding	Government
Healthcare Regulation	Strict	Healthcare Funding	Government	Healthcare Technology	Advanced
Healthcare Funding	Government	Healthcare Technology	Advanced	Healthcare Policy	Universal
Healthcare Technology	Advanced	Healthcare Policy	Universal	Healthcare Regulation	Strict
Healthcare Policy	Universal	Healthcare Regulation	Strict	Healthcare Funding	Government
Healthcare Regulation	Strict	Healthcare Funding	Government	Healthcare Technology	Advanced
Healthcare Funding	Government	Healthcare Technology	Advanced	Healthcare Policy	Universal
Healthcare Technology	Advanced	Healthcare Policy	Universal	Healthcare Regulation	Strict
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Healthcare Funding	Government	Healthcare Technology	Advanced	Healthcare Policy	Universal

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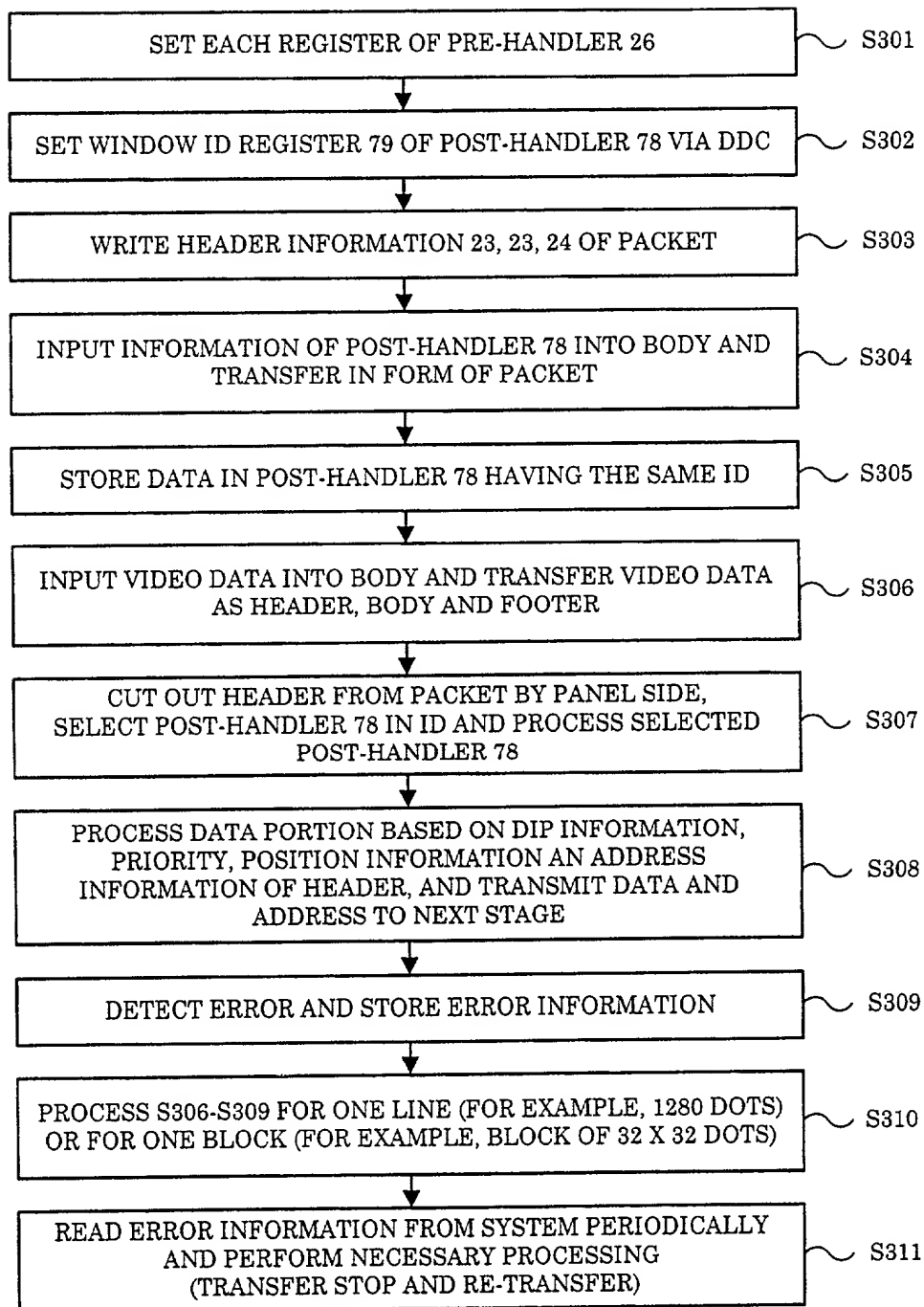
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FIG. 5



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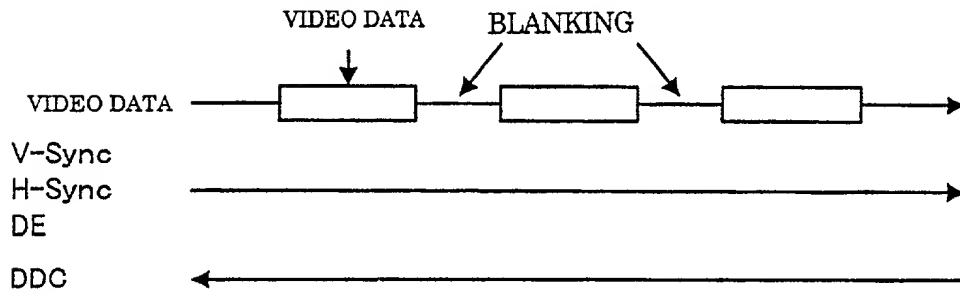
FIG. 6



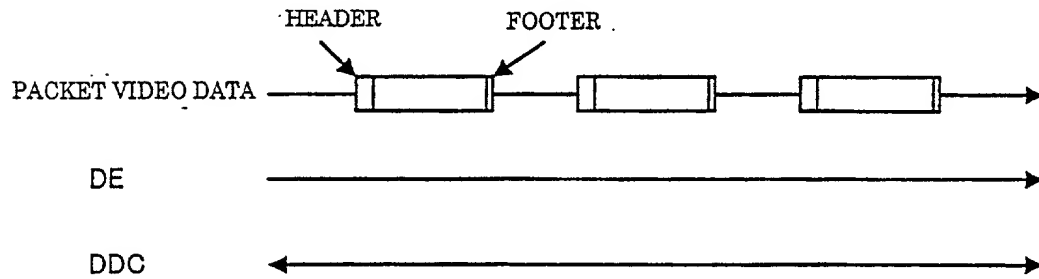
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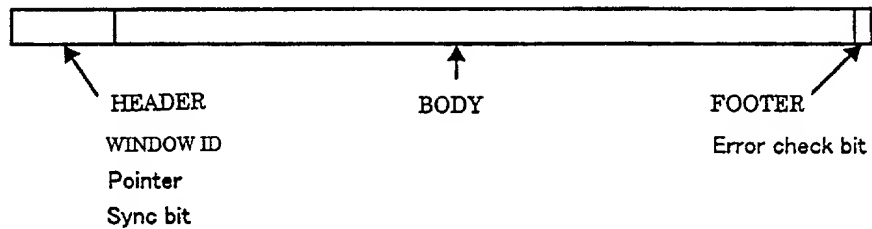
FIG. 7



(a) CONVENTIONAL TRANSFER OF VIDEO DATA



(b) TRANSFER OF VIDEO DATA IN THIS EMBODIMENT



(c) FORMAT OF PACKET VIDEO DATA

FIG. 8

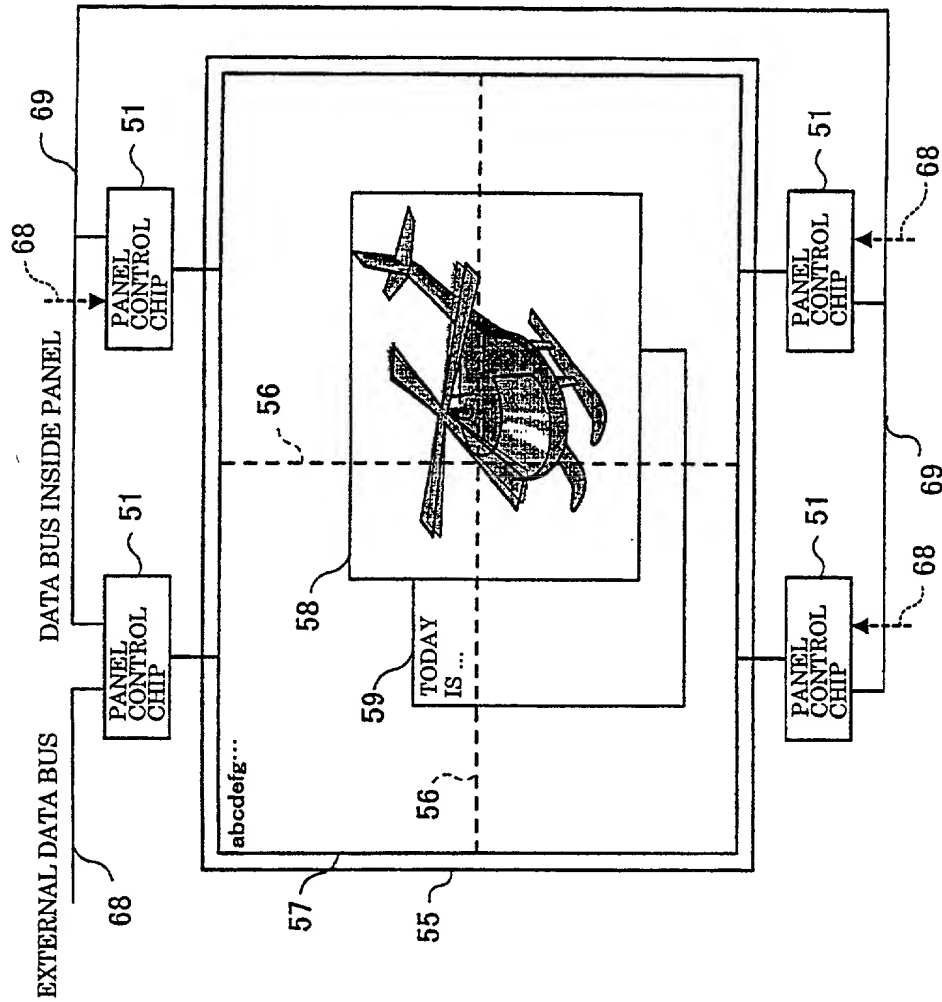
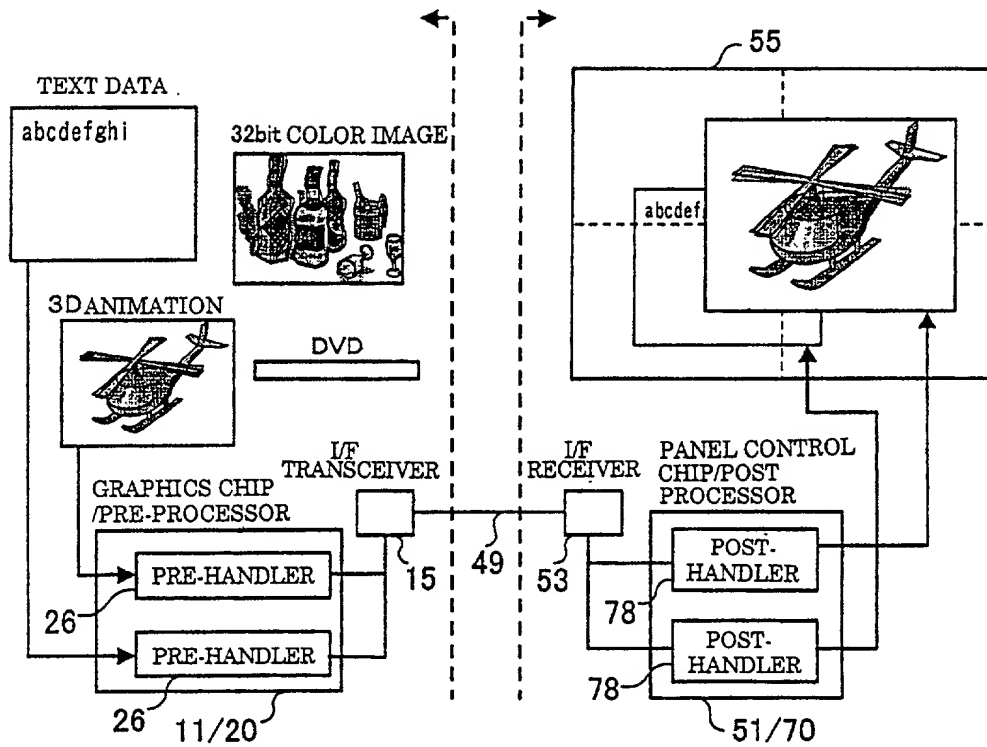
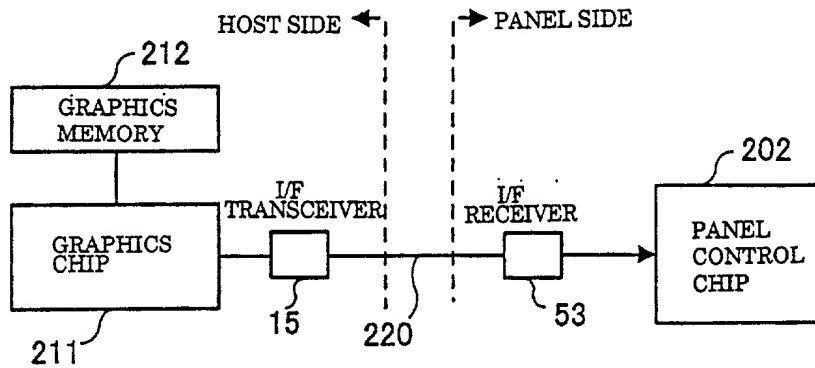


FIG. 9



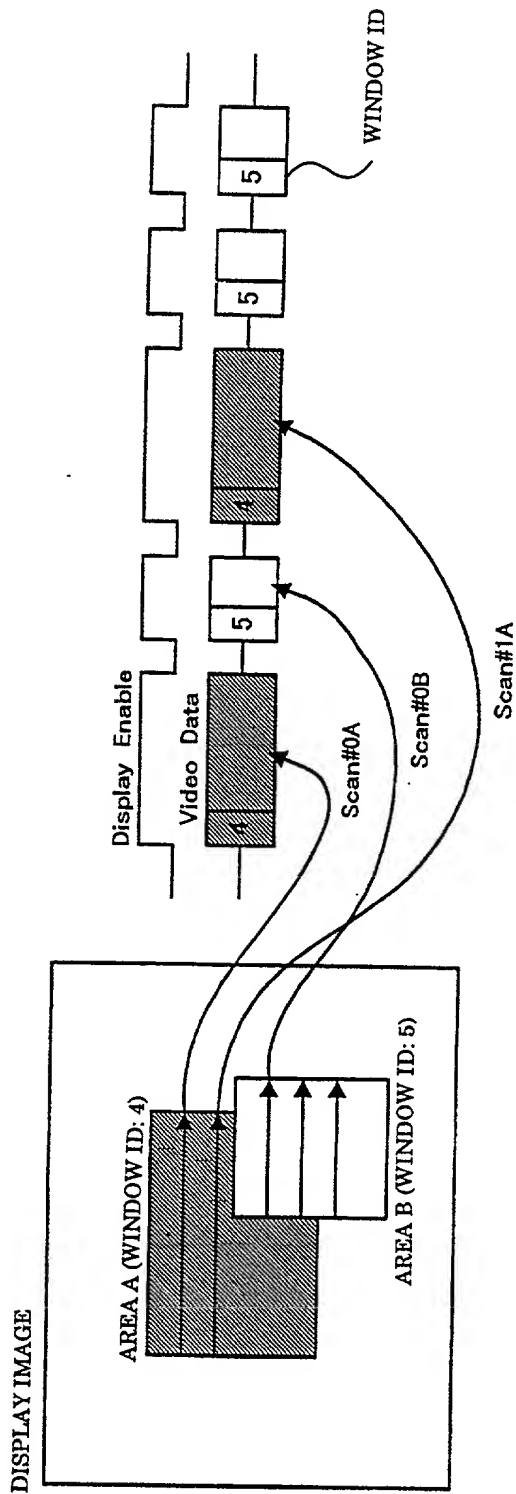
(a) DATA SOURCE AND PROCESSING SYSTEM



(b) LIMITATION OF DATA BAND WIDTH

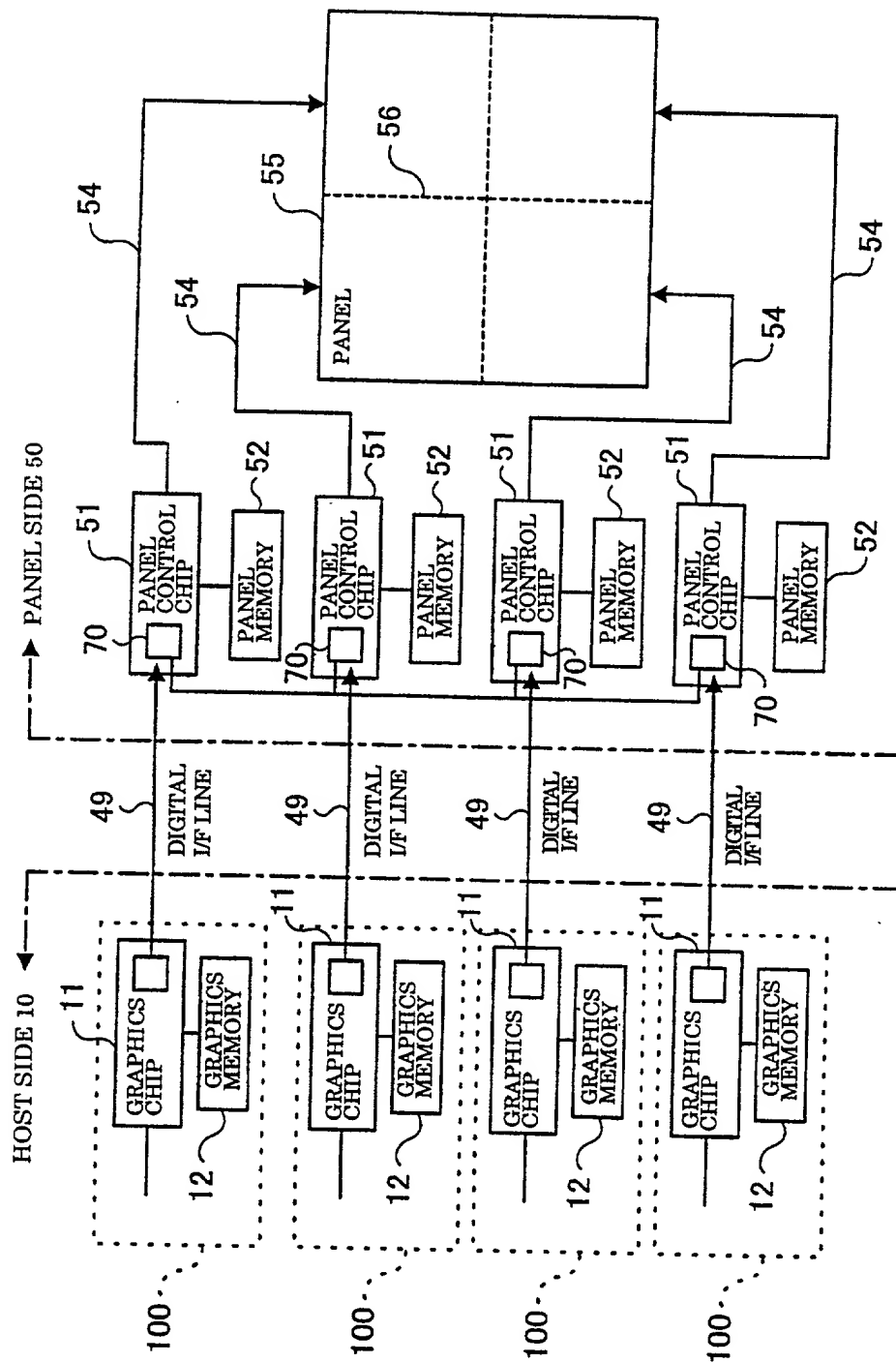
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FIG. 10



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FIG. 11



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The diagram illustrates a graphics system architecture with two main components: a Graphics Chip/Pre-processor (40) and a Panel Control Chip/Post Processor (50), connected via a DDC (Display Data Channel) line.

Graphics Chip/Pre-processor (40):

- Synchronization Control Circuit (43):** Contains an Offset Register (41), an Adder (42), and a Multiplexer (43). It receives H-Sync and Host Side 20 signals.
- Vertical Synchronization Counter (44):** Receives Host Side 20 and provides output to the Multiplexer (43) and the Readweight Control (45).
- Readweight Control (45):** Receives Host Side 20 and provides output to the Job No. Output Register (33).
- Registers (33, 34):** Job No. Output Register (33) and Job No. Input Register (34).
- DDC Handler (37):** Receives DDC signals and provides output to the Job No. Output Register (33) and the Job No. Input Register (34).

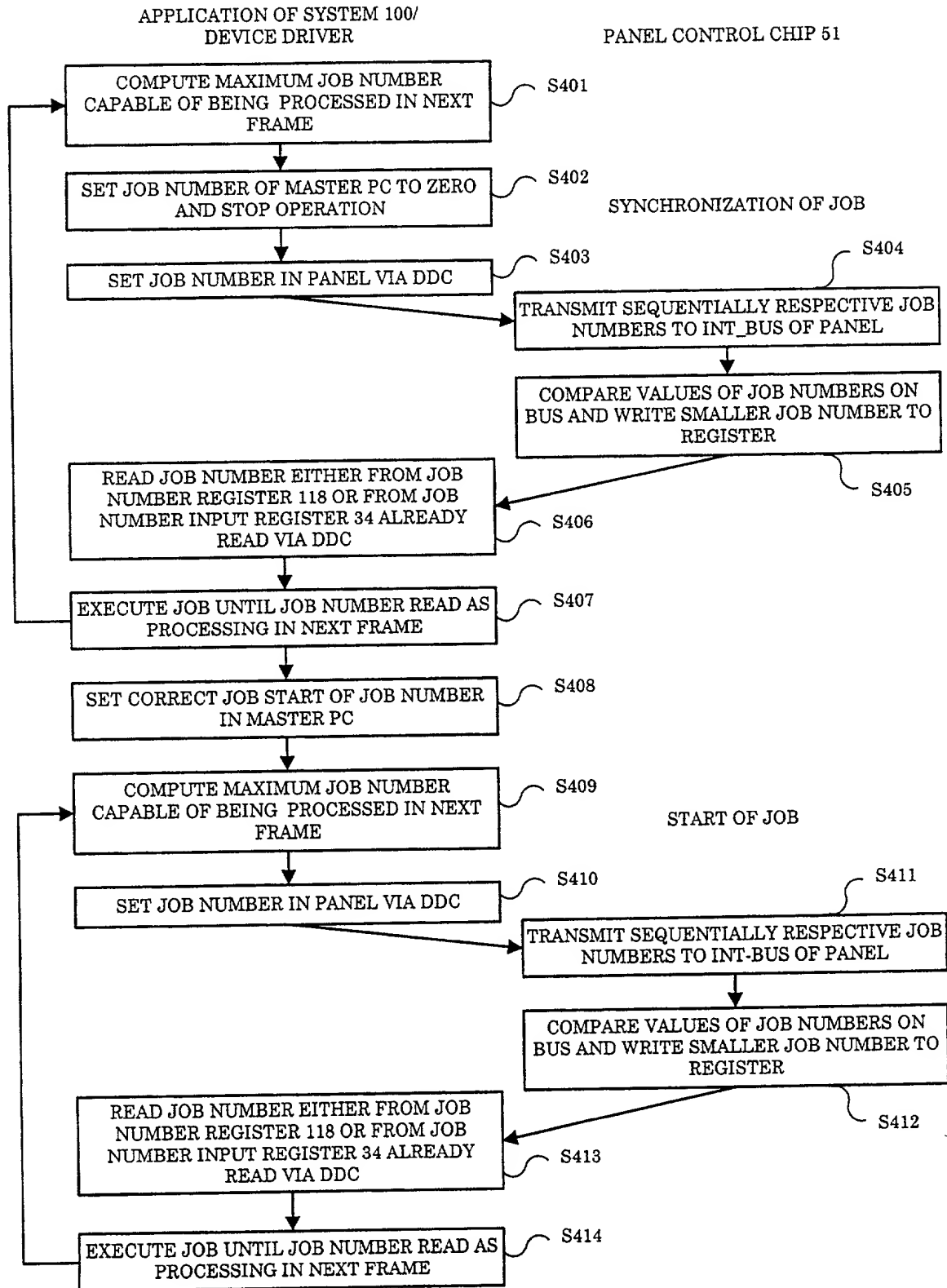
Panel Control Chip/Post Processor (50):

- Synchronization Control Circuit (114):** Contains an Offset Register (113), an Adder (114), and a Vertical Synchronization Counter (112). It receives INT_HSync and INT_VSync signals.
- Vertical Synchronization Counter (112):** Receives INT_VSync and provides output to the Adder (114) and the DDC Handler (115).
- DDC Handler (115):** Receives DDC signals and provides output to the Job No. Input Register (116) and the Job No. Output Register (117).
- Registers (116, 117, 118, 119):** Job No. Input Register (116), Job No. Output Register (117), Job No. Input Register (118), and Job No. Output Register (119).
- Comparator (120):** Receives output from the Job No. Output Register (117) and the Job No. Input Register (118).
- INT_Bus (121):** Receives output from the Comparator (120).

Connections:

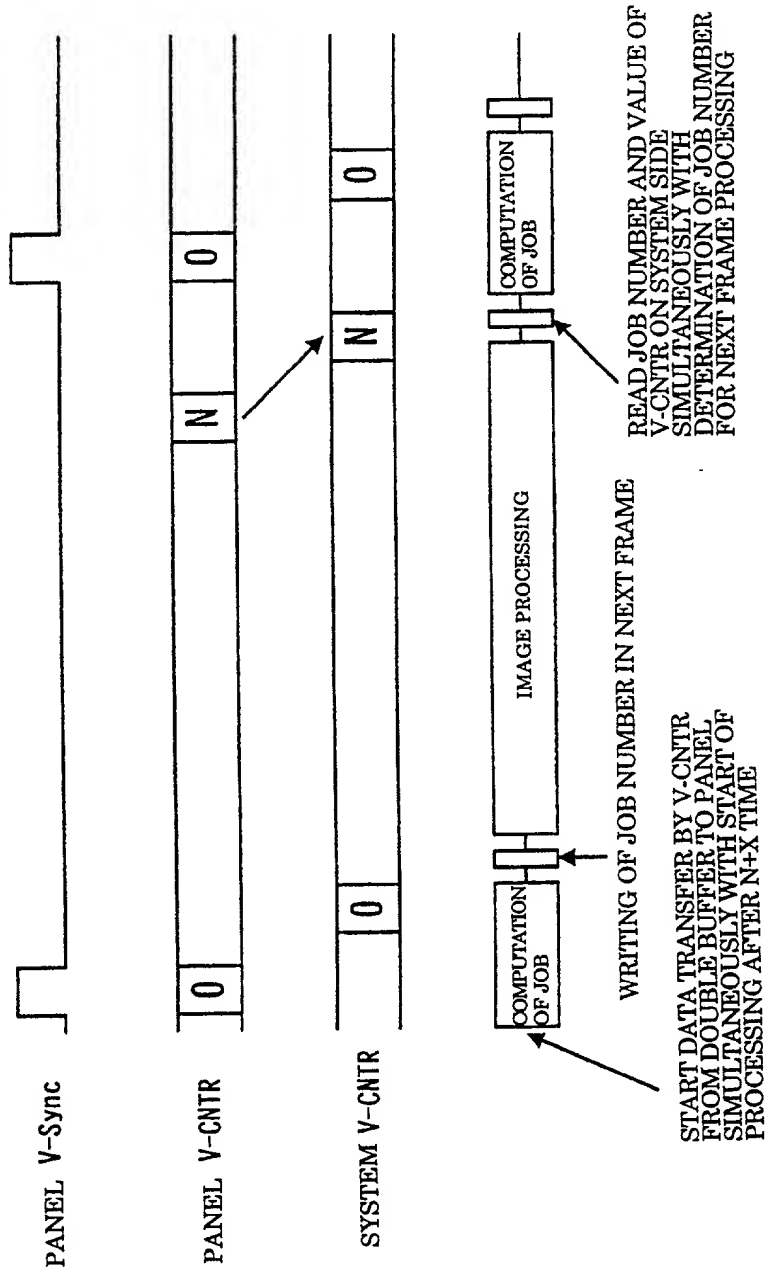
- Host Side 10:** Input to the Graphics Chip/Pre-processor (40).
- Host Side 20:** Input to the Graphics Chip/Pre-processor (40).
- Panel Side 50:** Input to the Panel Control Chip/Post Processor (50).
- Panel Side 60:** Input to the Panel Control Chip/Post Processor (50).
- DDC:** Bidirectional communication line between the DDC Handler (37) and the DDC Handler (115).
- INT_HSync:** Input to the Panel Control Chip/Post Processor (50).
- INT_VSync:** Input to the Panel Control Chip/Post Processor (50).
- INT_Bus:** Output from the Panel Control Chip/Post Processor (50).

FIG. 13



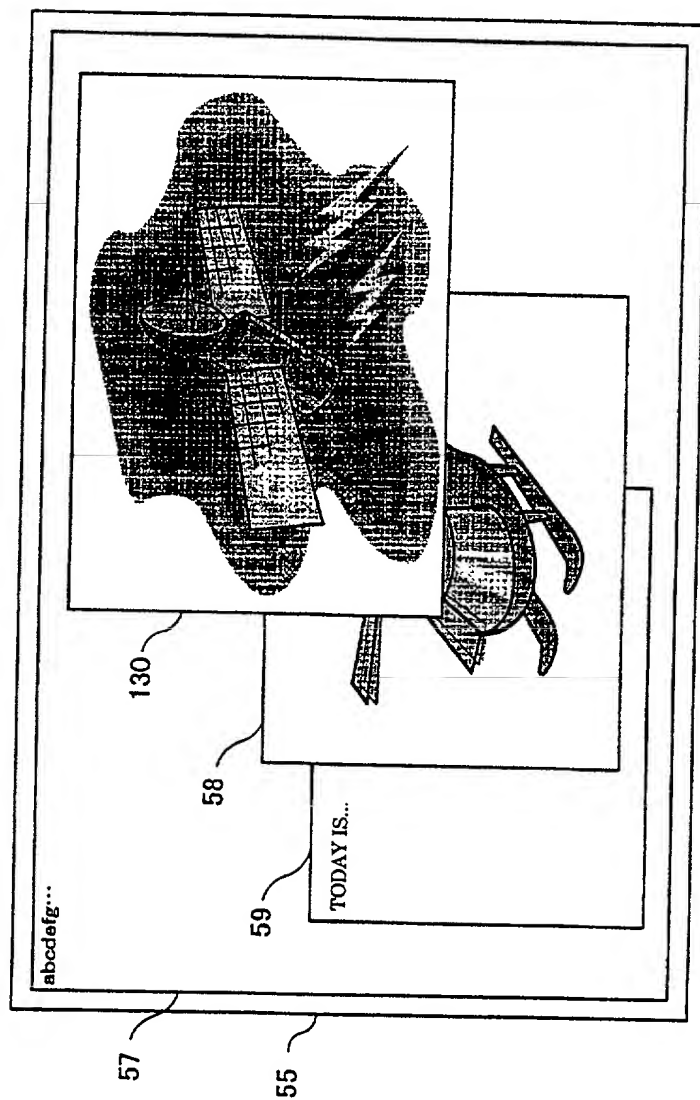
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FIG. 14



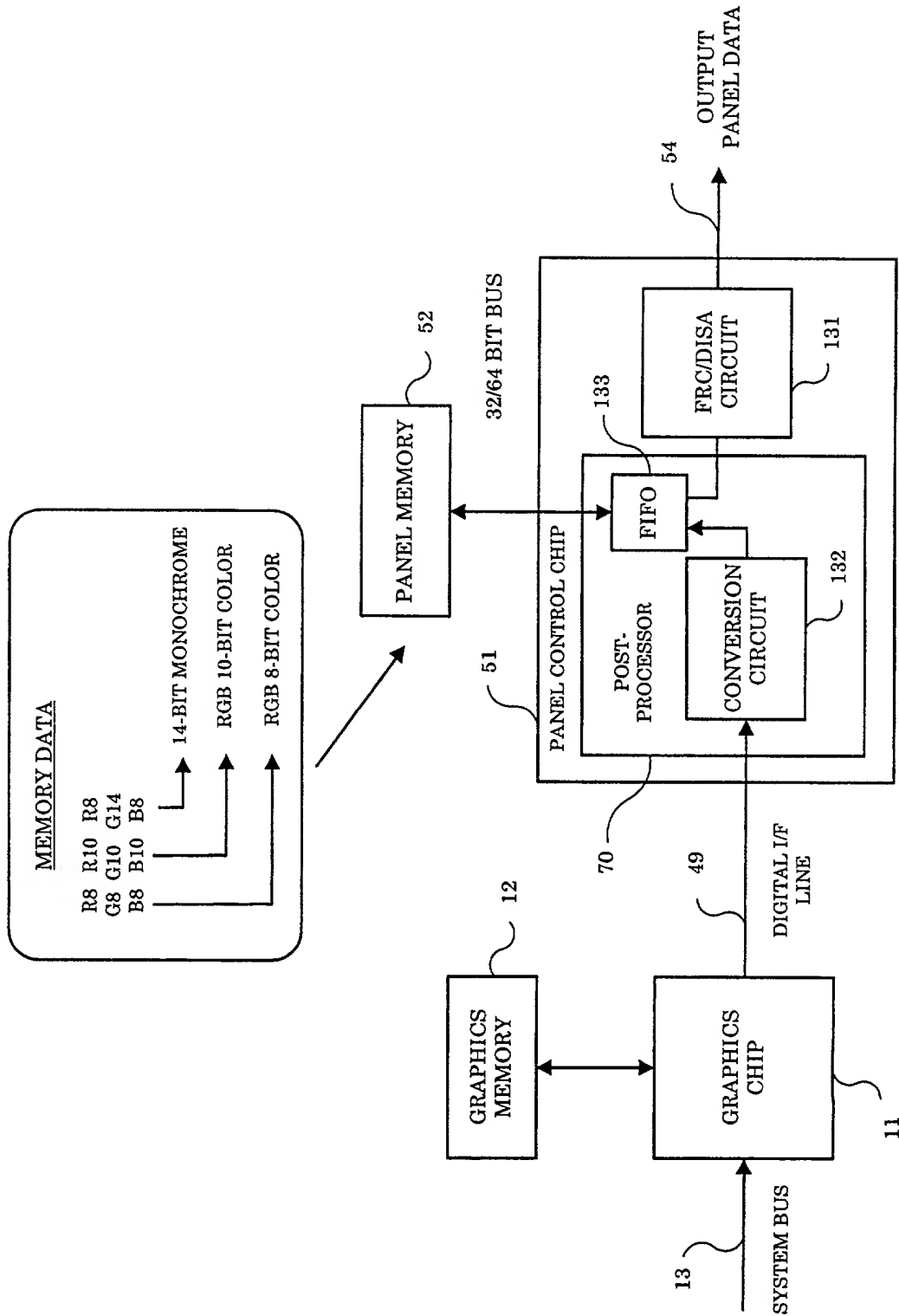
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FIG. 15



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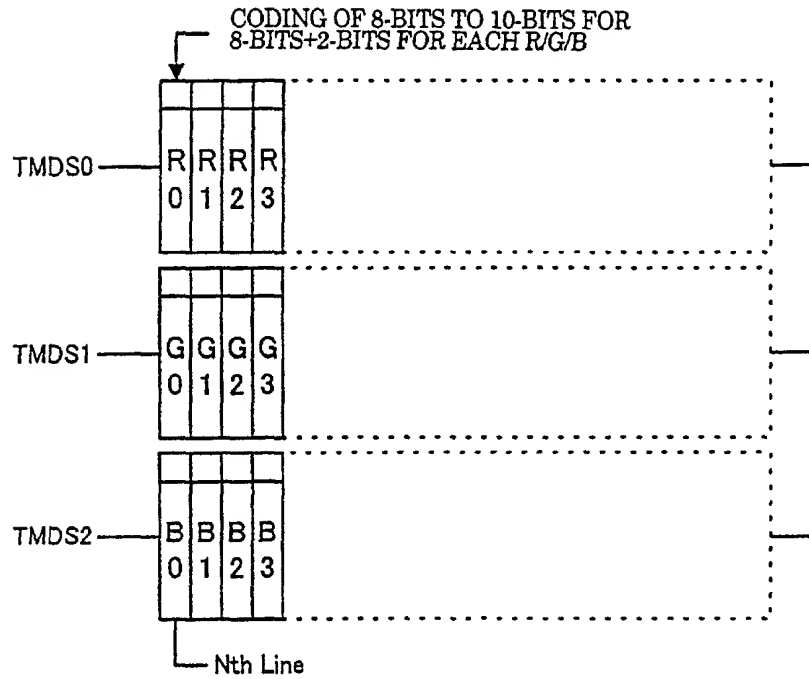
FIG. 16



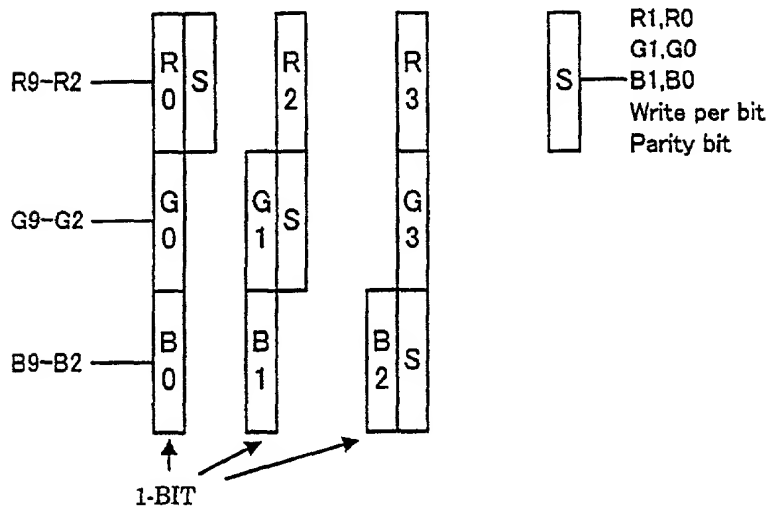
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FIG. 17



(a) TMDS DATA TRANSFER



(b) BIT ASSIGN OF 30-BIT COLOR

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FIG. 18

